In the Claims:

Please amend the claims as follows:

Claim 1 (currently amended): An array substrate for a liquid crystal display device, comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating film covering the gate electrode;

an active layer overlapping the gate electrode over the gate insulating film;

an ohmic contact layer on a part of the active layer, the ohmic contact layer defining a channel region in the active layer;

a drain electrode at an upper portion of the substrate, the drain electrode including, at least in part, two layers of conductive materials and having a first drain contact hole penetrating the two layers;

a protective layer over the drain electrode, the protecting layer having a second drain contact hole communicating with the first drain contact hole; and

a pixel electrode over the protective layer, the pixel electrode contacting the drain electrode at inner surfaces of the first drain contact hole formed in the drain electrode through the second drain contact hole,

wherein the gate insulating film is exposed through the first and second drain contact holes, and

wherein the pixel electrode directly contacts the exposed gate insulating film through the first and second drain contact holes.

Claim 2 (currently amended): The array substrate according to claim 1, wherein [[the]] a width of the second drain contact hole is larger than or substantially equal to that of the first drain contact hole.

Claim 3 (currently amended): The array substrate according to claim 1, wherein said two layers of conductive materials [[are]] includes a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 4 (currently amended): The array substrate according to claim 1, further comprising:

a gate line, connected to the gate electrode, over the substrate for receiving a scanning signal;

a data line crossing the data line for receiving a data signal;

~~a gate electrode connected to the gate line;~~

~~a gate insulating film covering the gate line and the gate electrode;~~

~~an active layer overlapping the gate electrode over the gate insulating film;~~

~~an ohmic contact layer on a part of the active layer, the ohmic contact layer defining a channel region in the active layer;~~ and

a source electrode connected to the data line, the source electrode and said drain electrode being absent over the channel region and being in contact with the ohmic contact layer[[;]].

Claim 5 (currently amended): The array substrate according to claim 4, wherein said two layers [[are]] includes a first metal layer and a second metal layer on the first metal layer, and

wherein the first metal layer and the ~~ohmic contact~~ second metal layer ~~thereunder~~ have substantially the same pattern.

Claim 6 (original): The array substrate according to claim 4, further comprising:

a data pad at one end of the data line over the substrate, the data pad including, at least in part, said two layers of conductive materials, the data pad having a first data contact hole penetrating the two layers; and

a data pad terminal electrode over the protective layer,

wherein the protective layer is situated over the data pad, and has a second data contact hole communicating with the first data contact hole, and

wherein the data pad terminal electrode contacts the data pad at the inner surfaces of the first data contact hole formed in the data pad through the second data contact hole.

Claim 7 (currently amended): The array substrate according to claim 6, wherein [[the]] a width of the second data contact hole is larger than or substantially equal to that of the first data contact hole.

Claim 8 (currently amended): The array substrate according to claim 6, wherein said two layers of conductive materials of the data pad [[are]] include a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 9 (original): The array substrate according to claim 6, wherein the data pad is over the gate insulating film.

Claim 10 (currently amended): The array substrate according to claim 9, wherein said two layers of the data pad [[are]] includes a first metal layer and a second metal layer on the first metal layer, and

wherein the data pad further includes a semiconductor layer beneath the first metal layer.

Claim 11 (original): The array substrate according to claim 10, wherein the first metal layer of the two layers of the data pad and the underlying semiconductor layer have substantially the same pattern.

Claim 12 (withdrawn): A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a gate electrode and a gate line over a substrate;

forming a gate insulating film over the substrate;

forming a semiconductor layer over the gate insulating film;

forming a data line, a source electrode, and a drain electrode over the gate insulating film, each of the data line, the source electrode, and the drain electrode including, at least in part, two layers of conductive materials, the step including removing portions of at least one of the two layers to pattern the drain electrode and, at the same time, define a first drain contact hole penetrating the two layers;

forming a protective layer over the gate insulating film, the data line, the source electrode, and the drain electrode, the protective layer having a second drain contact hole communicating with the first drain contact hole; and

forming a pixel electrode over the protective layer, the pixel electrode contacting the drain electrode at inner surfaces of the first drain contact hole formed in the drain electrode through the second drain contact hole.

Claim 13 (withdrawn): The method according to claim 12, wherein the width of the second drain contact hole is lager than or substantially equal to that of the first drain contact hole.

Claim 14 (withdrawn): The method according to claim 12, wherein said two layers of conductive materials are a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 15 (withdrawn): The method according to claim 12, wherein the step of forming the semiconductor layer includes the steps of:

forming an active layer overlapping the gate electrode over the gate insulating film; and

forming an ohmic contact layer on a part of the active layer,

wherein said two layers of conductive materials are a first metal layer and a second metal layer on the first metal layer, and

wherein the first metal layer of said two layers of the drain electrode and the ohmic contact layer thereunder have substantially the same pattern.

Claim 16 (withdrawn): The method according to claim 12, further comprising the steps of:

forming a data pad at one end of the data line, the data pad including, at least in part, said two layers of conductive materials, the step including removing portions of at least one of the two layers to pattern the data pad and, at the same time, define a first data contact hole penetrating the two layers, the data pad being situated below the protective layer;

removing a portion of the protective layer to define a second data contact hole communicating with the first data contact hole; and

forming a data pad terminal electrode over the protective layer, the data pad terminal electrode being in contact with the data pad at inner surfaces of the first data contact hole formed in the data pad through the second data contact hole.

Claim 17 (withdrawn): The method according to claim 16, wherein the width of the second data contact hole is lager than or substantially equal to that of the first data contact hole.

Claim 18 (withdrawn): The method according to claim 16, wherein said two layers of conductive materials are a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 19 (withdrawn): The method according to claim 16, wherein the data pad is formed over the gate insulating film.

Claim 20 (withdrawn): The method according to claim 19, wherein said two layers are a first metal layer and a second metal layer on the first metal layer, and

wherein the data pad further includes a semiconductor layer beneath the first metal layer.

Claim 21 (withdrawn): The method according to claim 20, wherein the first metal layer of the two layers of the data pad and the underlying semiconductor layer have substantially the same pattern.

Claim 22 (new): An array substrate for a liquid crystal display device, comprising:

a substrate;

a gate electrode formed on the substrate;

a gate insulating film covering the gate electrode;

an active layer overlapping the gate electrode over the gate insulating film;

an ohmic contact layer on a part of the active layer, the ohmic contact layer defining a channel region in the active layer;

a drain electrode at an upper portion of the substrate, the drain electrode including, at least in part, two layers of conductive materials and having a first drain contact hole penetrating the two layers and the ohmic contact layer;

a protective layer over the drain electrode, the protecting layer having a second drain contact hole communicating with the first drain contact hole; and

a pixel electrode over the protective layer, the pixel electrode contacting the drain electrode at inner surfaces of the first drain contact hole formed in the drain electrode through the second drain contact hole,

wherein the active layer is exposed through the first and second drain contact holes, and

wherein the pixel electrode directly contacts the exposed active layer through the first and second drain contact holes.

Claim 23 (new): The array substrate according to claim 22, wherein a width of the second drain contact hole is larger than or substantially equal to that of the first drain contact hole.

Claim 24 (new): The array substrate according to claim 22, wherein said two layers of conductive materials include a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 25 (new): The array substrate according to claim 22, further comprising:

a gate line, connected to the gate electrode, over the substrate for receiving a scanning signal;

a data line crossing the data line for receiving a data signal; and

a source electrode connected to the data line, the source electrode and said drain electrode being absent over the channel region and being in contact with the ohmic contact layer.

Claim 26 (new): The array substrate according to claim 25, wherein said two layers include a first metal layer and a second metal layer on the first metal layer, and

wherein the first metal layer and the ohmic contact layer thereunder have substantially the same pattern.

Claim 27 (new): The array substrate according to claim 25, further comprising:

a data pad at one end of the data line over the substrate, the data pad including, at least in part, said two layers of conductive materials, the data pad having a first data contact hole penetrating the two layers; and

a data pad terminal electrode over the protective layer,

wherein the protective layer is situated over the data pad, and has a second data contact hole communicating with the first data contact hole, and

wherein the data pad terminal electrode contacts the data pad at inner surfaces of the first data contact hole formed in the data pad through a second data contact hole.

Claim 28 (new): The array substrate according to claim 27, wherein a width of the second data contact hole is larger than or substantially equal to that of the first data contact hole.

Claim 29 (new): The array substrate according to claim 27, wherein said two layers of conductive materials of the data pad includes a first metal layer and a second metal layer on the first metal layer, the first metal layer being one of molybdenum (Mo), chrome (Cr), tantalum (Ta), Tungsten (W), and titanium (Ti), and the second metal layer being aluminum (Al) or an aluminum alloy.

Claim 30 (new): The array substrate according to claim 27, wherein the data pad is over the gate insulating film.

Claim 31 (new): The array substrate according to claim 30, wherein said two layers of the data pad include a first metal layer and a second metal layer on the first metal layer, and

wherein the data pad further includes a semiconductor layer beneath the first metal layer.

Claim 32 (new): The array substrate according to claim 31, wherein the first metal layer of the two layers of the data pad and the underlying semiconductor layer have substantially the same pattern.